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Patent Application of: Christophe J. Chevallier

Title: CMOS IMAGER WITH INTEGRATED NON-VOLATILE MEMORY

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PATENT APPLICATION TRANSMITTAL

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CMOS IMAGER WITH INTEGRATED NON-VOLATILE MEMORY

Technical Field of the Invention

The present invention relates generally to image sensing devices and in particular to a complementary metal oxide semiconductor (CMOS) imager with integrated non-volatile memory.

Background of the Invention

With the advent of multimedia communications, there arises the need for low-cost solid state imagers to complement communication devices and computers. An image input sensor is central to any teleconferencing and multimedia application and is used to convert an optical image focused on the sensor into electrical signals. The image input sensor typically includes an array of light detecting elements where each element produces a signal corresponding to the intensity of light impinging on that element when an image is focused on the array. These signals may then be used, for example, to display a corresponding image on a monitor or to help record information about the optical image, as performed by a digital camera.

A common type of image sensor is a charge coupled device (CCD). CCDs have dominated vision applications because of their superior dynamic range, low fixed-pattern noise and high sensitivity to light. However, CCD technology is quite complex, suffers from low yields, and is expensive due to specialized processing involved to produce such devices. Moreover, integrating analog/digital convertors and digital processing with a CCD array on the same chip is not feasible. As a result, multiple chip sets are required to accommodate the CCD array image sensor and the required logic and processing circuitry. An imaging sensing device having a multiple chip set package is more costly to produce than a device utilizing a single chip set. Other well known disadvantages exist for CCDs.

In comparison, image sensor research has advanced pure complementary metal oxide semiconductor (CMOS) image sensors. CMOS image sensors consist of photodiodes or phototransistors that are used as the light detecting elements where the conductivity of the elements correspond to the intensity of light impinging on the elements. CMOS image sensors have a great cost advantage over CCDs of similar resolution. This is due to the fact that CMOS image sensors have high yields because they are fabricated by the same semiconductor foundries that make computer memory chips, digital signal processors, analog/digital convertors, etc.

CMOS image sensors address many of the shortcomings of CCDs. CMOS technology allows the fabrication of a single chip set having image capture capability along with logic and processing capabilities including analog/digital conversion and digital signal processors. Memory such as RAM and ROM can also be integrated onto the same single chip set. However, integrating non-volatile memory onto the same circuit as a CMOS imager presents a problem due to the non-volatile memory's sensitivity to light. Most non-volatile memory cells rely on a trapped charge stored on a floating gate in a field effect transistor (FET). Erasure of the trapped charge from the floating gate is performed by exposure to ultraviolet light.

As a consequence, current image devices, such as digital cameras, do not place non-volatile memory on the same integrated circuit as the CMOS image sensor. Separating the CMOS imager from non-volatile memory results in an image sensing device having a multiple chip set package which adds to the cost of the device. In addition, the size of the image sensing device is directly related to the required number of chip sets. If non-volatile memory were integrated onto the same integrated circuit as a CMOS imager, then a more compact image sensing device could be achieved.

Therefore, what is needed is a single integrated circuit having a CMOS imager and peripheral components for receiving and processing a received image, including non-volatile memory integrated onto the same integrated circuit. For the reasons stated above, and for other reasons stated below which will become apparent

to those skilled in the art upon reading and understanding the present specification, there is a need in the art to provide a CMOS imager with integrated non-volatile memory wherein light received by the image sensor does not effect the non-volatile memory.

Summary of the Invention

A CMOS imager and non-volatile memory are integrated on a single integrated circuit wherein a layer of protective material covers the non-volatile memory for blocking light received by the imager. Logic and support circuitry are also fabricated on the integrated circuit for decoding and processing optical information received by the CMOS imager.

In one embodiment, an image sensor on an integrated circuit is presented wherein the integrated circuit comprises a CMOS imager for defining an image, non-volatile memory for storing the image and/or program code information, and logic and support circuitry are fabricated on the integrated circuit such that a level of protective material covers the non-volatile memory for blocking light received by the CMOS imager. The level of protective material is a metal or opaque material provided as part of the fabrication process. A method of fabricating a CMOS imager on an integrated circuit with non-volatile memory is also presented.

CMOS technology allows the fabrication of a single chip set having image capture, analog/digital conversion, digital processing and image storing capabilities. Image storing capabilities eliminates the need for placing non-volatile memory on a separate chip to protect it from the light received by the CMOS imager. Further, a single chip set allows a lower cost imaging device. In addition, an imaging device comprising a single chip set is more compact in size as compared to a multiple chip set imaging device.

Therefore, integrating non-volatile memory onto the same substrate as a CMOS imager which captures optical information, including logic and support circuitry for decoding and processing this information, allows a single chip set to replace a multiple chip set imaging device performing the same function. In

different embodiments of the invention a protective layer of varying scope is described for blocking light received by the CMOS imager, wherein the protective layer is a metal or opaque material provided as part of the fabrication process. Further embodiments of the invention will become apparent by reference to the drawings and by reading the following detailed description.

Brief Description of the Drawings

Figure 1 is a block diagram of an embodiment of a digital camera system utilizing a CMOS imager with integrated non-volatile memory according to the teachings of the present invention;

Figure 2 is an embodiment of a typical architecture for a CMOS imager; and

Figures 3 is a plan views of an integrated circuit having a CMOS imager along with non-volatile memory covered by a protective layer according to the teachings of the present invention.

Detailed Description of the Preferred Embodiment

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the inventions may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present inventions is defined only by the appended claims.

The terms wafer and substrate used in the following description include any structure having an exposed surface with which to form the integrated circuit (IC) structure of the invention. The term substrate is understood to include semiconductor wafers. The term substrate is also used to refer to semiconductor structures during processing, and may include other layers that have been fabricated

thereupon. Both wafer and substrate include doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures well known to one skilled in the art. The term conductor is understood to include semiconductors, and the term insulator is defined to include any material that is less electrically conductive than the materials referred to as conductors.

The present invention, in one embodiment, is a single integrated circuit having a complementary metal oxide semiconductor (CMOS) imager for capturing optical information, logic circuitry to decode and process the information and non-volatile memory for storing the optical information and/or program code, wherein the non-volatile memory is covered by a protective layer for blocking light received by the CMOS imager. The protective layer can be a metal or opaque material provided as part of the fabrication process of the integrated circuit. The present invention thus allows non-volatile memory to be placed on the same integrated circuit as the CMOS imager without having the light received by the CMOS imager adversely effecting stored data. A digital camera system utilizing the CMOS imager is first described, wherein the digital camera system serves as an alternate embodiment of the present invention. An architecture of the CMOS imager is also presented along with a general layout, or floorplan, of a single substrate having the CMOS imager, non-volatile memory and processing capabilities integrated thereon.

Figure 1 is a block diagram of an embodiment of a single chip 3 digital camera system 5 utilizing a CMOS imager 14 with integrated non-volatile memory 34 according to the teachings of the present invention. There are several different techniques used to make digital cameras 5, wherein the techniques provide for different quality cameras covering a variety of applications. These techniques are well known in the art and the invention is not limited to any particular digital camera type.

Referring to Figure 1, light 8 representing an image passes through a lens 10 that is controlled by a stop 12 and shutter (not shown). The light 8 is photoelectrically converted by the CMOS imager 14, which is an image pick-up

device for generating and outputting an analog image signal photoelectrically converted from an image incident thereon. CMOS imagers 14 are well known to one skilled in the art and the present invention is not limited to any particular type of CMOS imager.

The analog image signal from the CMOS imager 14 is converted by an analog/digital (A/D) convertor 16 to be recorded in a frame memory 18. The writing and reading of image data in and out of the frame memory 18 are controlled by a memory controller 20 under the control of a micro-controller 22. The digital image data read out from the frame memory 18 is coupled to a digital signal processor (DSP) 24. An output from the DSP 24 is converted into an analog image signal by a digital/analog (D/A) convertor 26. The analog image signal is supplied to an output terminal 28 and an electronic view finder 30 for viewing.

Video data that is read out of the frame memory 18 is subjected to a compression process in a data compression/decompression unit 32 conforming to a compression standard, such as Joint Pictures Expert Group (JPEG). Other compression standards well known to one skilled in the art are acceptable, such as wavelet compression. Unlike Fourier and cosine transforms for compression, Wavelet compression consists of transforming signals into a sum of small, overlapping waves for analyzing, storing and transmitting information.

The compressed image data is fed to a memory unit 34 to be recorded. Memory unit 34 comprises non-volatile memory so that if power is removed from the camera 5 the data contents remain in the memory cells that make up the non-volatile memory unit 34. Non-volatile memory includes, but is not limited to, EPROM, EEPROM and flash memory.

In lieu of utilizing non-volatile memory for storing images, the non-volatile memory in, one embodiment, could be used to store program code information while the images can be stored in a in a battery backed up RAM (not shown). In one embodiment, the code is firmware for controlling a digital signal processor 24 or the micro-controller 22. Also included within the firmware are control of other

parameters that effect the digital camera 5, such as specific sensitivities of the imager field, a camera identification number, or additional parameters.

Most non-volatile memory cells rely on a trapped charge stored on a floating gate in an FET. The charge reaches the floating gate either by tunneling or avalanche injection from a region near the drain. Erasure of the charge from a floating gate is made by tunneling or by exposure to ultraviolet light. Unless the memory unit 34 is protected from the light 8 received by the CMOS imager, data stored on a floating gate within the memory unit 34 can be erased. Protection of the non-volatile memory unit 34 from light received by the CMOS imager 14 is described in more detail with reference to Figure 3. In another embodiment, the non-volatile memory cells store a charge at an interface of two layers of oxide. For purposes of the invention, a memory cell which stored data between oxide layers is considered equivalent to a floating gate.

In playback, the video image that is read out from the memory unit 34 is recorded in the frame memory 18. The video data that is read out from the frame memory 18 is, like in the previous case, fed through the DSP 24 and another D/A convertor 26 for viewing via the electronic view finder 30 or via a monitor coupled to the output terminal 28.

The frame memory 18 is controlled by a memory controller 20 which is operated according to the micro-controller 22. The micro-controller 22 also controls the data compressing/decompressing unit 32, memory controller 20, and the memory unit 34.

A switch 40 is coupled to the micro-controller 22 for providing information regarding the operation of the digital camera 5. The switch 40 comprises a plurality of individual switches. For instance, a trigger 41 switch is provided for instructing exposure operation, a plus 42 and a minus 43 switch for selecting an image in a play-back operation, a record/play 44 switch for instructing recording and play-back operation. Other switches allow for control of the mode of the camera such a high-speed mode 45, a low-speed mode 46 and a normal speed mode 47. The digital camera 5 is not limited to the above described switches and one skilled in the art

realizes other switching options applicable to the digital camera 5 depicted in Figure 1. An LCD 50 displays the camera operation state under control of the micro-controller 22.

The micro-controller 22 receives and outputs data through data bus 52 to control the entire digital camera 5 operation. The recording of the extracted image in the memory unit 34 is made through the control of the micro-controller 22. An image received by the CMOS imager 14 is produced by extracting the digital image data from the frame memory 18 and storing this image in the memory unit 34. Interface circuitry 53 is also coupled to the data bus for communicating the image data to another device, such as a printer, a computer, or even a memory card. In one embodiment, interface circuitry 53 is a PCMIA interface.

An embodiment of a CMOS image sensor 14, of the present invention, is illustrated in Figure 2. The CMOS imager 14 is a solid state imaging device that depends on a photovoltaic response when silicon is exposed to light 8. Photons in the visible and near-IR regions of the spectrum have sufficient energy to break covalent bonds in the silicon. The number of electrons released is proportional to the intensity of the light 8 received from an image. The CMOS image sensor 14 can comprise a photodiode array 80, a vertical shift register 82, a horizontal shift register 84, an array controller 86, a video output unit 88 and other support circuits.

One embodiment of the photodiode array 80 comprises 800 horizontal pixels by 1000 vertical pixels. The image format is generally less because the non-image lines provide color characterization and reference information. Support circuits for the photodiode array 80 constitute the rest of the CMOS imager 14. A vertical shift register 82 controls reset, integrate and readout cycle for each line of the array 80. A horizontal shift register 84 controls column readout. A two-way serial interface and internal register (not shown) provide control, monitoring and several operating modes for the camera functions.

CMOS pixel-array 80 construction uses active or passive pixels. Active pixel sensors can be photodiode or photogate pixels and include amplification circuitry in each pixel. Passive pixels use a photodiode to collect the photocharge.

A passive pixel comprises a photodiode in which the photon energy converts to free electrons and comprises an access transistor to a column bus. After photocharge integration, an array controller 86 turns on the access transistor. The charge transfers to the capacitance of the column bus, where the charge integrating amplifier at the end of the bus senses the resulting voltage. The column bus voltage resets the photodiode and the array controller 86 turns off the access transistor. The pixel is then ready for another integration period.

The passive photodiode pixel achieves high "quantum efficiency." Quantum efficiency is a ratio of photon-generated electrons that the pixel captures to the photons incident on the pixel area. A low fill factor reduces quantum efficiency wherein the fill factor is a ratio of light-sensitive area to the pixel's total size, also known as aperture efficiency.

An active photogate pixel utilizes a charge-transfer technique to enhance the array's 80 image quality. The active circuitry then performs a doubling-sampling readout. First, the array controller 86 resets the output diffusion, and a source-follower buffer reads the voltage. Then a pulse on the photogate and access transistor transfers the charge voltage. This correlated double-sampling technique enables fast readout and mitigates fixed pattern noise and reset noise at the source.

Independent of utilizing active or passive pixels, the output of the array 80 is an analog image signal photoelectrically converted from an image incident thereon which then passes through a video output unit 88 before reaching the A/D convertor 16 illustrated in Figure 1.

Figure 3 is plan view of an integrated circuit 100 having a CMOS imager 14 and non-volatile memory 34 which is covered by a protective layer. In Figure 3, a protective layer 102 covers the non-volatile memory 34 so that light received by the CMOS imager 14 does not effect data stored within the memory cells. Other circuits fabricated onto the single integrated circuit 3 can include the micro-controller 22, an A/D convertor 16, a D/A convertor 26 and a DSP 24. Logic support circuitry 108 is also fabricated onto the circuit 100, wherein the logic circuitry 108 comprises the remainder of the functions necessary for the digital

camera 5 to operate. Logic circuitry 108 components are collectively referred to as peripheral support for the CMOS imager 14 and the non-volatile memory unit 34.

In one embodiment the protective layer 102 (in addition to covering the non-volatile memory 34) is a metal layer used as an interconnect for electrically connecting other areas of the integrated circuit 100. That is, one of the metal layers used to connect circuitry of the integrated circuit is not patterned over the memory cells and provides an opaque protective layer. In another embodiment the protective layer is an opaque material utilized by the imager 14 for blocking light in between the pixels. Thus, the opaque material provided for the imager is, likewise, used to provide a memory protection layer. This opaque material can be, but is not limited to, metal. For example, the opaque material can be polyamide. Because the non-volatile memory 34 is susceptible to light, the protective layer 102 serves to block exposure to light received by the imager 14. Even though the protective layer 102 primarily serves to block light from reaching the non-volatile memory 34, the protective layer 102 can be utilized to cover the other components integrated on the substrate 110 to minimize the build up of heat resulting from the received light.

Fabrication processes for the CMOS integrated circuit 100 closely resemble those of fabricating microprocessors and ASICs because of the similar diffusion and transistor structures. Several metal layers are optimal for producing image sensor 14. One of these metal layers can be utilized as the protective layer 102.

A difference between CMOS image sensor processes and advanced microprocessor and ASIC processes is that the decreasing feature size works well for logic circuits but does not benefit pixel construction. Smaller pixels mean lower light sensitivity and dynamic range. Even though the logic circuits can be made smaller, the photosensitivity area can shrink only so far before diminishing the benefits of less silicon area.

Each single integrated circuit 100 is fabricated upon a monolithic substrate 110. In one embodiment, the substrate 110 is a bulk semiconductor, such as P-silicon. In another embodiment, an epitaxial substrate 110 is used.

Conclusion

A CMOS imager 14 and non-volatile memory 34 integrated onto a single substrate 110 along with logic and support circuitry for decoding and processing optical information received by the CMOS imager 14 has been described. A protective layer 102 covers the non-volatile memory 34 contained on the substrate 110 for blocking light received by the CMOS imager 14. In one embodiment the protective layer 102 is a metal layer which can also be used as an interconnect layer for electrically connecting other circuits on the substrate 110. In another embodiment the protective layer 102 is an opaque layer formed during the fabrication process of the integrated circuit 100. Integrating a CMOS imager 14, non-volatile memory 34 and support circuitry for decoding and processing optical information received by the CMOS imager 14 allows for a single chip 3 image sensing device, such as a digital camera 5.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those skilled in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment of the present invention. This application is intended to cover any adaptations or variations of the present invention.

What is claimed is:

1. An image sensor fabricated on a substrate comprising:

a CMOS image sensor for defining an image signal photoelectrically converted in response to received light;

an array of non-volatile memory cells for receiving and storing the image signal, wherein each memory cell stores a trapped charge; and

a level of protective material fabricated over the array of non-volatile memory cells for blocking the light received by the CMOS imager so that the trapped charged is not erased from exposure to the light.

2. The image sensor of claim 1 wherein each memory cell is a field effect transistor with a floating gate.

3. The image sensor of claim 1 wherein the level of protective material is polyamide.

4. The image sensor of claim 1 wherein the level of protective material is fabricated as part of the CMOS imager.

5. The image sensor of claim 1 wherein the level of protective material is a layer of metal fabricated as an interconnect for electrically connecting the CMOS imager and other circuits on the substrate.

6. The image sensor of claim 1 wherein the CMOS imager comprises an active pixel array.

7. The image sensor of claim 1 wherein the CMOS imager comprises a passive pixel array.

8. An image sensor on an integrated circuit comprising:

a CMOS imager for defining an image in response to received light;

a non-volatile memory unit for storing the image, wherein the non-volatile memory unit is fabricated adjacent to the CMOS imager; and

a level of protective material fabricated over the non-volatile memory for blocking the light received by the CMOS imager.

9. The image sensor of claim 8 wherein the level of protective material is fabricated as part of the CMOS imager.

10. The image sensor of claim 8 further comprising a micro-controller for controlling transfer of the image from the CMOS imager to the non-volatile memory unit.

11. The image sensor of claim 10 wherein the non-volatile memory stores program code information for controlling the microcontroller.

12. The image sensor of claim 8 further comprising a digital signal processor for receiving and processing the image from the CMOS imager.

13. The image sensor of claim 8 wherein the level of protective material is a layer of metal.

14. The image sensor of claim 8 wherein the layer of metal is fabricated as an interconnect for electrically connecting the CMOS imager and other circuits on the substrate.

15. An image sensor on an integrated circuit comprising:

a CMOS imager for defining an image in response to received light;

a microcontroller for controlling the CMOS imager;

a non-volatile memory unit fabricated adjacent to the CMOS imager for storing program code or data; and

a level of protective material fabricated over the non-volatile memory for blocking the light received by the CMOS imager.

16. The image sensor of claim 15 wherein the non-volatile memory receives and stores the image.

17. The image sensor of claim 15 wherein the level of protective material is metal fabricated as an interconnect layer for electrically connecting other circuits on the single integrated circuit.

18. The image sensor of claim 15 further comprising a digital signal processor for receiving and processing the image from the CMOS imager.

19. A digital camera fabricated on a single integrated circuit comprising:

a CMOS image sensor for defining an analog image signal photoelectrically converted in response to received light;

an analog to digital convertor for receiving and converting the analog image signal into a digital image signal;

a frame memory for recording the digital image signal;

a data compression/decompression unit for compressing the digital image signal provided by the frame memory;

a non-volatile memory unit for receiving the compressed digital image signal, wherein a layer of protective material is fabricated over the non-volatile memory unit for blocking the light received by the CMOS imager; and

a microcontroller for controlling the exchange of the digital image signal between the frame memory and the non-volatile memory unit.

20. The digital camera of claim 19 further comprising:

a digital signal processor for receiving and processing the digital image signal from the frame memory;

a digital to analog convertor for converting the digital image signal to an analog image signal, wherein the digital signal processor and the digital to analog convertor are fabricated on the single integrated circuit; and

an electronic view finder for viewing the image.

21. The digital camera of claim 19 wherein the non-volatile memory unit is fabricated adjacent to the CMOS imager sensor.

22. The digital camera of claim 19 wherein the protective layer is fabricated as part of the CMOS imager sensor.

23. The digital camera of claim 19 wherein the non-volatile memory unit stores program code information for controlling the microcontroller.

24. The digital camera of claim 19 wherein the protective layer is fabricated as a metal interconnect layer for electrically connecting circuits on the integrated circuit.

25. The digital camera of claim 19 wherein the CMOS imager comprises an active pixel array.

26. The digital camera of claim 19 wherein the CMOS imager comprises a passive pixel array.

27. A method of fabricating a CMOS imager on an integrated circuit with non-volatile memory comprising the steps of:

fabricating an array of non-volatile memory cells;

fabricating a light blocking layer over the non-volatile memory cells; and

fabricating the CMOS imager for defining an image in response to received light.

28. The method of claim 27 wherein the light blocking layer is a metal layer used as an interconnect for electrically connecting other circuits on the integrated circuit.

Abstract of the Disclosure

A CMOS imager and non-volatile memory are integrated on a single substrate along with logic and support circuitry for decoding and processing optical information received by the CMOS imager. A protective layer covers the non-volatile memory contained on the substrate for blocking light received by the CMOS imager. The protective layer can be a metal layer used as an interconnect over other areas of the substrate or an opaque layer provided during the fabrication process. Integrating a CMOS imager, non-volatile memory and peripheral circuitry for decoding and processing optical information received by the CMOS imager allows for a single chip image sensing device, such as a digital camera.

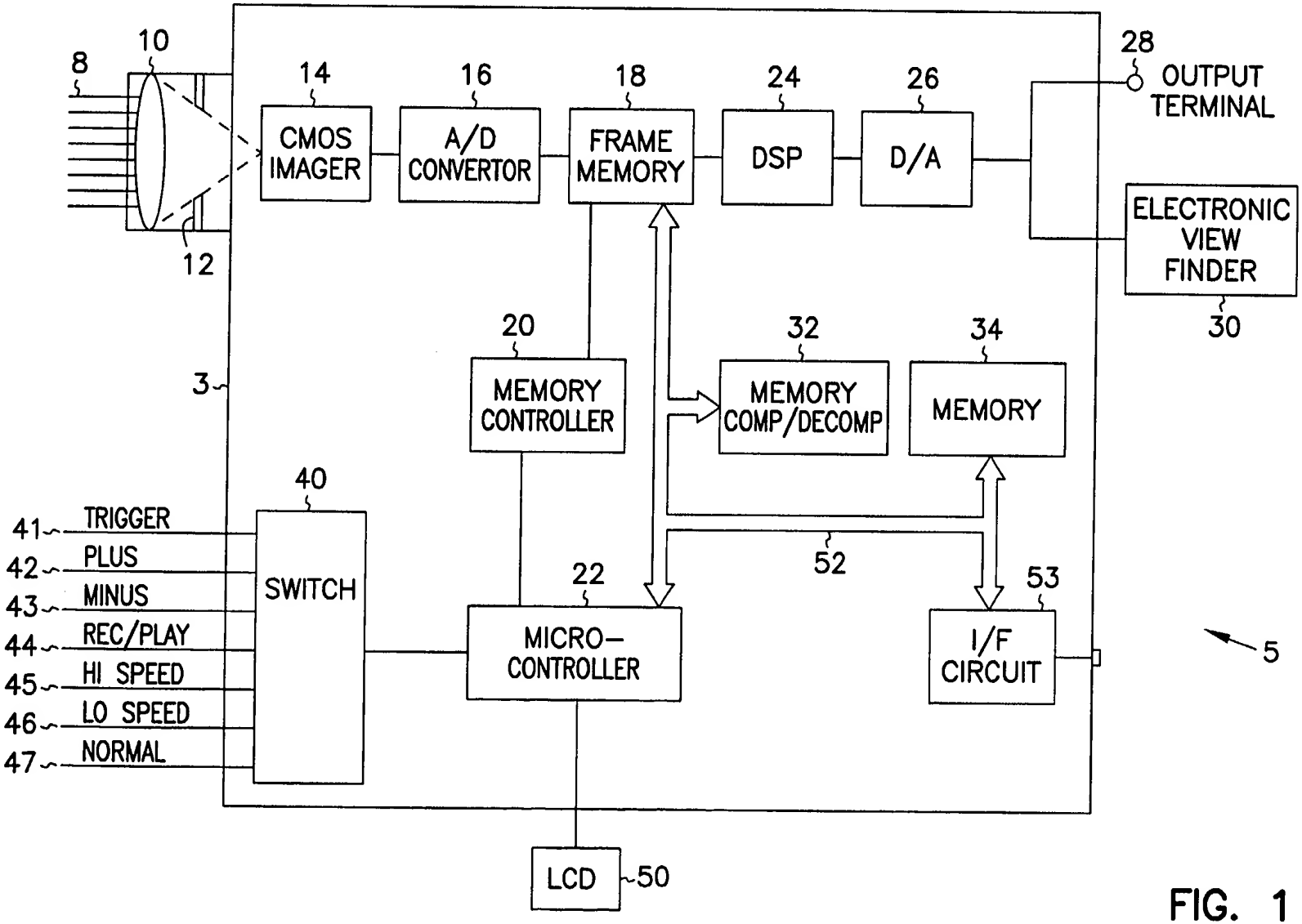

FIG. 1

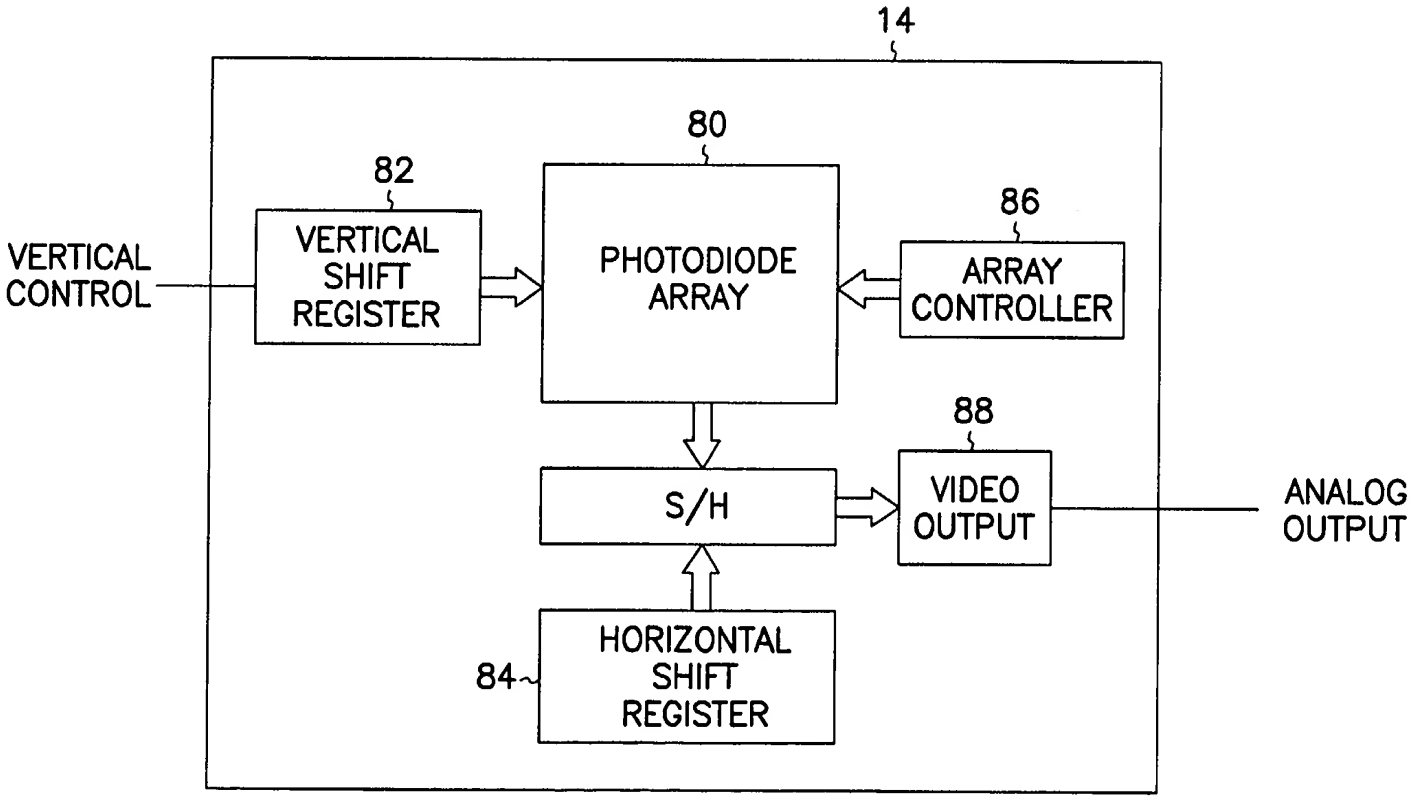

FIG. 2

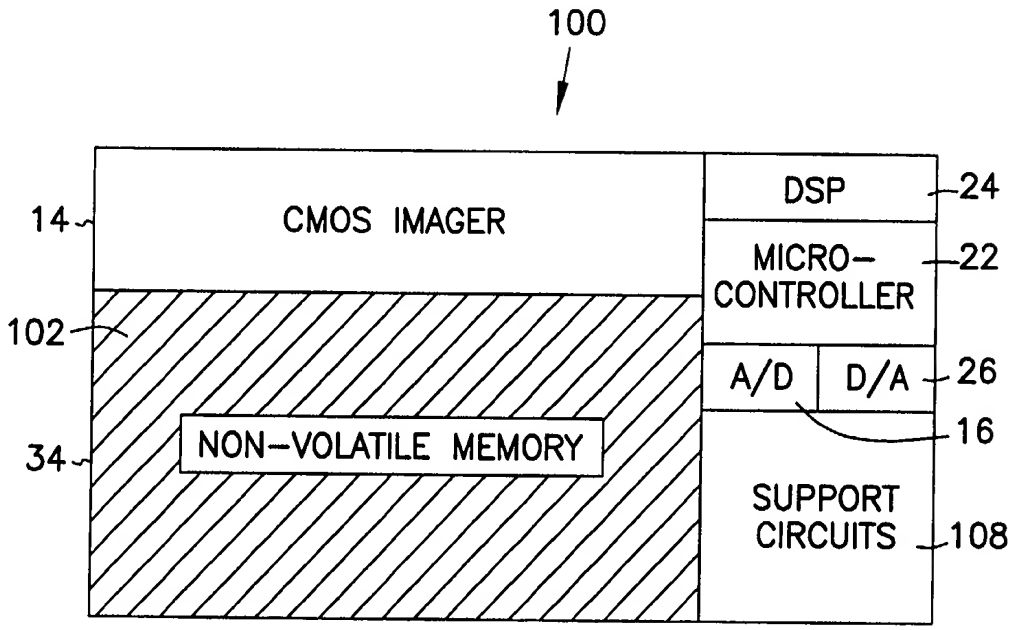

FIG. 3

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

DECLARATION FOR PATENT APPLICATION

As a below named inventor I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

CMOS IMAGER WITH INTEGRATED NON-VOLATILE MEMORY .

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (see page 3 attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, §119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

No such applications have been filed.

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

No such applications have been filed.

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application.

No such applications have been filed.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Christophe J. Chevallier

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
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Signature: _____ Date: _____

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§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) it establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) it refutes, or is inconsistent with, a position the applicant takes in:

(i) opposing an argument of unpatentability relied on by the Office, or

(ii) asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

S/N Unknown **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Christophe J. Chevallier	Examiner: Unknown	
Serial No.:	Unknown	Group Art Unit: Unknown	
Filed:	Herewith	Docket: 703.032US1	
Title:	CMOS IMAGER WITH INTEGRATED NON-VOLATILE MEMORY		

POWER OF ATTORNEY BY ASSIGNEE AND CERTIFICATE BY ASSIGNEE UNDER 37 CFR § 3.73(b)

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Micron Technology, Inc., assignee of the entire right, title and interest in the above-identified application by assignment attached hereto, hereby appoints the attorneys and agents of the firm of SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A., listed as follows:

Anglin, J. Michael	Reg. No. 24,916	Forrest, Bradley A.	Reg. No. 30,837	Litman, Mark A.	Reg. No. 26,390
Arora, Suneel	Reg. No. P-42,267	Hale, Jeffrey D.	Reg. No. 40,012	Lundberg, Steven W.	Reg. No. 30,568
Bernkopf, Paul A.	Reg. No. P-41,615	Harris, Robert J.	Reg. No. 37,346	McCrackin, Ann M.	Reg. No. P-42,858
Bianchi, Timothy E.	Reg. No. 39,610	Hofmann, Rudolph P., Jr.	Reg. No. 38,187	Polglaze, Daniel J.	Reg. No. 39,801
Billion, Richard E.	Reg. No. 32,836	Holloway, Sheryl S.	Reg. No. 37,850	Provence, David L.	Reg. No. P-43,022
Brennan, Thomas F.	Reg. No. 35,075	Huebsch, Joseph C.	Reg. No. P-42,673	Schwegman, Micheal L.	Reg. No. 25,816
Brooks, Edward J., III	Reg. No. 40,925	Klima-Silberg, Catherine I.	Reg. No. 40,052	Simboli, Paul B.	Reg. No. 38,616
Clark, Barbara J.	Reg. No. 38,107	Kluth, Daniel J.	Reg. No. 32,146	Slifer, Russell D.	Reg. No. 39,838
Drake, Eduardo E.	Reg. No. 40,594	Lacy, Rodney L.	Reg. No. 41,136	Terry, Kathleen R.	Reg. No. 31,884
Dryja, Michael A.	Reg. No. 39,662	Leffert, Thomas W.	Reg. No. 40,697	Viksnins, Ann S.	Reg. No. 37,748
Embretson, Janet E.	Reg. No. 39,665	Lemaire, Charles A.	Reg. No. 36,198	Woessner, Warren D.	Reg. No. 30,440
Fogg, David N.	Reg. No. 35,138				

and also attorneys Michael L. Lynch (Reg. No. 30,871) and Lia M. Pappas (Reg. No. 34,095) of Micron Technology, Inc., as its attorneys with full power of substitution to prosecute this application and to transact all business in the Patent and Trademark Office in connection therewith.

The assignee certifies that the above identified assignment has been reviewed and to the best of the assignee's knowledge and belief, title is in the assignee.

Please direct all correspondence regarding this application to the following:

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Dated: June 11, 1998

MICRON TECHNOLOGY, INC.

By: _____

Name: Michael L. Lynch

Title: Chief Patent Counsel